CENTRAL FAX CENTER
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**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (previously presented): An apparatus comprising:

a memory unit comprising a memory location to store a first data value;

a processing unit to generate an address value corresponding to the memory location;

a buffer unit to store at least a portion of the first data value and to provide at least a portion of the first data value to the processing unit in response to the address value being generated;

buffer logic to determine whether at least a portion of the first data value stored in the buffer unit corresponds to the address value based on, at least in part, detection of an overflow signal.

Claim 2 (original): The apparatus of claim 1, wherein at least a portion of the first data value is to be provided to the processing unit from the buffer unit instead of at least a portion of the first data value stored in the memory unit.

Claim 3 (canceled)

Claim 4 (previously presented): The apparatus of claim 1 wherein the buffer logic comprises overflow detection logic to detect whether an overflow occurs with regard to an address computation based on the overflow signal.

Claim 5 (previously presented): The apparatus of claim 1 wherein the buffer logic comprises an arithmetic unit to increment or decrement the address value.

Claim 6 (previously presented): The apparatus of claim 1 further comprising invalidation logic to invalidate data stored in the buffer unit if a write operation is addressed to the memory location.

Claim 7 (original): The apparatus of claim 1 wherein the memory unit is a cache memory.

Claim 8 (original): The apparatus of claim 7 further comprising a plurality of buffer units to store data stored within a plurality of locations within the cache memory.

Claim 9 (currently amended): A processor comprising:

a cache memory to store a plurality of data;

a processor core to generate addresses corresponding to data stored within the cache memory;

a plurality of buffers from which the processor core may retrieve copies of data stored within the cache memory, the plurality of buffers being associated with a plurality of locations within the cache memory, wherein the plurality of buffers are present within ~~the cache memory~~ a memory controller coupled to the processor core.

Claim 10 (original): The processor of claim 9 further comprising a selection unit to select one of the plurality of buffers from which to retrieve data.

Claim 11 (original): The processor of claim 10 further comprising alignment and signing logic to appropriately shift and apply appropriate sign information to data stored within the buffer selected by the selection unit.

Claim 12 (original): The processor of claim 9 further comprising a buffer control unit to detect whether an address generated by the processor core corresponds to data stored within any of the plurality of buffers, and if so, to select data within the plurality of buffers to which the address generated by the processor core corresponds.

Claim 13 (currently amended): The processor of claim 12 further comprising validation indicators to indicate whether data stored within the ~~load~~ plurality of buffers is valid.

Claim 14 (previously presented): The processor of claim 13 wherein the validation indicators are to indicate that data within all of the buffers are invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which any of the buffers correspond.

Claim 15 (previously presented): The processor of claim 13 wherein the validation indicators are to indicate that data within a buffer is invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which the buffer corresponds.

Claim 16 (previously presented): The processor of claim 15 further comprising a plurality of tag storage units to store portions of a cache memory address to which the buffers correspond.

Claim 17 (original): The processor of claim 16 further comprising a comparator unit to compare contents of the tag storage unit to a portion of a cache memory address generated by the processor core.

Claims 18-33 (canceled)

Claim 34 (currently amended): A processor comprising:

a cache memory to store a plurality of data;

a processor core to generate addresses corresponding to data stored within the cache memory;

a plurality of buffers from which the processor core is to retrieve copies of data stored within the cache memory, the plurality of buffers associated with a plurality of locations within the cache memory, wherein the copies of data are to be invalidated if a write operation is to occur to a cache memory location corresponding to any of the plurality of locations;

a buffer control unit to detect whether an address generated by the processor core corresponds to data stored within any of the plurality of buffers, and if so, to select data within the plurality of buffers to which the address generated by the processor core corresponds; and

validation indicators each to indicate whether data stored within the corresponding buffer is valid, wherein the validation indicators are to indicate that data within all of the buffers is invalid if the buffer control unit receives a clear signal from the processor core.

Claim 35 (previously presented): The processor of claim 34 further comprising a selection unit to select one of the plurality of buffers from which to retrieve data.

Claim 36 (previously presented): The processor of claim 35 further comprising alignment and signing logic to shift and apply sign information to data stored within the buffer selected by the selection unit.

Claims 37 - 39 (cancel)

Claim 40 (previously presented): An apparatus comprising:

a cache memory to store a plurality of data;

a processor core to generate addresses corresponding to data stored within the cache memory;

a buffer unit including:

a plurality of buffers to store copies of data stored within the cache memory;

a control unit coupled to the plurality of buffers including an adder to add a first or second value to a load address to form a modified address, and overflow logic to indicate if a corresponding buffer includes valid data based, at least in part, on an overflow signal from the adder.

Claim 41 (previously presented): The apparatus of claim 40 further comprising a plurality of tag storage units to store portions of a cache memory address to which the buffers correspond.

Claim 42 (previously presented): The apparatus of claim 41 further comprising a comparator unit to compare contents of the tag storage unit to a portion of a cache memory address generated by the processor core.

Claim 43 (previously presented): The apparatus of claim 40 wherein the control unit further comprises a selector to select either the modified address or a new address for storage in a first storage of the control unit.

Claim 44 (previously presented): The apparatus of claim 43 wherein the overflow logic is to indicate invalid data if the overflow signal is present and the processor core is in a first addressing mode.

Claim 45 (previously presented): The apparatus of claim 40 further comprising a validation indicator and a tag storage associated with each of the plurality of buffers to indicate

whether data stored within the corresponding buffer is valid, and a comparator to compare a tag stored in the tag storage with a portion of an address from the processor core, wherein the validation indicator is to be invalidated if the comparator indicates a match and the processor core has asserted a clear signal for the address.